IN THE SPECIFICATION

Please amend the paragraph beginning on page 1, line 6 as follows:

This application is a Divisional of U.S. Application No. 10/137,499 filed May 2, 2002, now U.S. Patent 7,045,430, which is incorporated herein by reference.

Please amend the paragraph beginning on page 1, line 8 as follows:

This application is related to the following, co-pending, commonly assigned applications, incorporated herein by reference:

U.S. Application Serial No. 10/081,439, now U.S. Patent 6,893,984, entitled: "Evaporated $LaAlO_3$ Films for Gate Dielectrics,"

U.S. Application Serial No. 10/137,058, entitled: "Atomic Layer Deposition and Conversion,"

U.S. Application Serial No. 10/137,168, entitled: "Atomic Layer of AlO_x for ULSI Gate Atomic Layer Deposition for Gate Dielectric Layer," and

U.S. Application Serial No. 09/797,324, now U.S. Patent 6,852,167, entitled: "Methods, Systems, and Apparatus for Uniform Chemical-Vapor Depositions."

Please delete the following paragraphs beginning on page 3, line 11 – page 5, line 11:

~~Summary of the Invention~~

~~A solution to the problems as discussed above is addressed in the present invention. In accordance with the present invention, a method of forming a gate dielectric on a transistor body region includes the atomic layer deposition of an amorphous film containing $LaAlO_3$ on the transistor body region. The ALD formation of the $LaAlO_3$ film is performed by pulsing a lanthanum containing precursor into a reaction chamber containing a substrate, pulsing a first oxygen containing precursor into the reaction chamber, pulsing an aluminum containing precursor into the reaction chamber, and pulsing a second oxygen containing precursor into the reaction chamber. Each precursor is pulsed into the reaction chamber for a selected time period. A length of time for pulsing each precursor is selected according to the precursor used. Between each precursor pulsing, precursor excess and reaction by products are removed from the reaction.~~

~~The $LaAlO_3$ film thickness is controlled by repeating for a number of cycles the pulsing of the lanthanum-containing precursor, the first oxygen-containing precursor, the aluminum-containing precursor, and the second oxygen-containing precursor until the desired thickness is formed.~~

~~A transistor is fabricated on a substrate by forming two source/drain regions separated by a body region, pulsing a $La(thd)_3$ (thd = 2,2,6,6- tetramethyl-3,5- heptanedione) source gas into a reaction chamber containing the substrate, pulsing ozone into the reaction chamber, pulsing a trimethylaluminium, $Al(CH_3)_3$, source gas into the reaction chamber, and pulsing water vapor into the reaction chamber. Controlling the processing temperatures, and the number of cycles of the lanthanum precursor and the number of cycles of the aluminum precursor provides the capability to form a film composition having a predetermined dielectric constant. A DMEAA, an adduct of alane (AlH_3) and dimethylehtylamine [$N(CH_3)_2(C_2H_5)$], source gas can be used in place of the trimethylaluminium source gas.~~

~~Advantageously, these methods can be used to further form a memory array where the process of forming the memory array is adapted to form gate dielectrics in accordance with the present invention. Additionally, an information handling system can be formed using the methods of the present invention, wherein a memory array fabricated in conjunction with fabricating a processor is formed to include transistors having gate dielectrics containing $LaAlO_3$. These gate dielectrics are formed by the ALD processing of a lanthanum sequence and a aluminum sequence for a number of cycles to provide a film containing $LaAlO_3$.~~

~~In accordance with the present invention, a transistor having two source/drain regions separated by a body region includes an amorphous gate dielectric containing $LaAlO_3$ located above the body region between the two source/drain regions. The gate dielectric may be essentially composed of $LaAlO_3$ or it may also contain Al_2O_3, and La_2O_3. Depending on its composition, the dielectric constant of the gate dielectric can range from about 9 to about 30. Depending on its composition, the gate dielectric can have a thickness corresponding to an equivalent oxide thickness (t_{eq}) in the range from about 1.5 Angstroms to about 5 Angstroms, in addition to larger t_{eq} values.~~

~~Advantageously, a memory array includes a number of transistors having two source/drain regions separated by a body region with an amorphous gate dielectric containing $LaAlO_3$ located above the body region between the two source/drain regions. These transistors~~

~~provide the memory array with an array of transistors having gate dielectrics with equivalent oxide thickness (t_{eq}) in the range from about 1.5 Angstroms to about 5 Angstroms, providing transistors operable at reduced voltage levels. Additionally, an information handling device, such as a computer, includes a processor and a memory array having a number of transistors with two source/drain regions separated by a body region that includes an amorphous gate dielectric containing $LaAlO_3$ located above the body region between the two source/drain regions.~~

~~These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.~~

Please insert the following paragraphs beginning on page 7, line 1:

In accordance with the present invention, a method of forming a gate dielectric on a transistor body region includes the atomic layer deposition of an amorphous film containing $LaAlO_3$ on the transistor body region. The ALD formation of the $LaAlO_3$ film is performed by pulsing a lanthanum containing precursor into a reaction chamber containing a substrate, pulsing a first oxygen containing precursor into the reaction chamber, pulsing an aluminum containing precursor into the reaction chamber, and pulsing a second oxygen containing precursor into the reaction chamber. Each precursor is pulsed into the reaction chamber for a selected time period. A length of time for pulsing each precursor is selected according to the precursor used. Between each precursor pulsing, precursor excess and reaction by-products are removed from the reaction. The $LaAlO_3$ film thickness is controlled by repeating for a number of cycles the pulsing of the lanthanum containing precursor, the first oxygen containing precursor, the aluminum containing precursor, and the second oxygen containing precursor until the desired thickness is formed.

A transistor is fabricated on a substrate by forming two source/drain regions separated by a body region, pulsing a $La(thd)_3$ (thd = 2,2,6,6- tetramethyl-3,5- heptanedione) source gas into a reaction chamber containing the substrate, pulsing ozone into the reaction chamber, pulsing a trimethylaluminium, $Al(CH_3)_3$, source gas into the reaction chamber, and pulsing water vapor

into the reaction chamber. Controlling the processing temperatures, and the number of cycles of the lanthanum precursor and the number of cycles of the aluminum precursor provides the capability to form a film composition having a predetermined dielectric constant. A DMEAA, an adduct of alane (AlH_3) and dimethylehtylamine [$N(CH_3)_2(C_2H_5)$], source gas can be used in place of the trimethylaluminium source gas.

Advantageously, these methods can be used to further form a memory array where the process of forming the memory array is adapted to form gate dielectrics in accordance with the present invention. Additionally, an information handling system can be formed using the methods of the present invention, wherein a memory array fabricated in conjunction with fabricating a processor is formed to include transistors having gate dielectrics containing $LaAlO_3$. These gate dielectrics are formed by the ALD processing of a lanthanum sequence and a aluminum sequence for a number of cycles to provide a film containing $LaAlO_3$.

In accordance with the present invention, a transistor having two source/drain regions separated by a body region includes an amorphous gate dielectric containing $LaAlO_3$ located above the body region between the two source/drain regions. The gate dielectric may be essentially composed of $LaAlO_3$ or it may also contain Al_2O_3, and La_2O_3. Depending on its composition, the dielectric constant of the gate dielectric can range from about 9 to about 30. Depending on its composition, the gate dielectric can have a thickness corresponding to an equivalent oxide thickness (t_{eq}) in the range from about 1.5 Angstroms to about 5 Angstroms, in addition to larger t_{eq} values.

Advantageously, a memory array includes a number of transistors having two source/drain regions separated by a body region with an amorphous gate dielectric containing $LaAlO_3$ located above the body region between the two source/drain regions. These transistors provide the memory array with an array of transistors having gate dielectrics with equivalent oxide thickness (t_{eq}) in the range from about 1.5 Angstroms to about 5 Angstroms, providing transistors operable at reduced voltage levels. Additionally, an information handling device, such as a computer, includes a processor and a memory array having a number of transistors with two source/drain regions separated by a body region that includes an amorphous gate dielectric containing $LaAlO_3$ located above the body region between the two source/drain regions.

Please amend the paragraph beginning on page 10, line 19 as follows:

In co-pending, commonly assigned U.S. patent applications: entitled "Evaporated $LaAlO_3$ Films for Gate Dielectrics," serial number 10/081,439, now U.S. Patent 6,893,984, $LaAlO_3$ is disclosed as a replacement for SiO_2 as material for forming gate dielectrics and other dielectric films in electronic devices such as MOS transistors. This application disclosed, among other things, forming layers of $LaAlO_3$ on silicon by electron beam evaporation of dry pellets of Al_2O_3 and La_2O_3 using two electron guns controlled by two rate monitors. Controlling the rates for evaporating the dry pellets of Al_2O_3 and La_2O_3 allows for the formation of a gate dielectric having a composition with a predetermined dielectric constant. The predetermined dielectric constant will range from the dielectric constant of Al_2O_3 to the dielectric constant of La_2O_3, depending on the composition of the film. Films substantially consisting of $LaAlO_3$ film could be obtained on silicon providing an amorphous dielectric layer with a dielectric constant between 21 and 24. Other reports indicate that $LaAlO_3$ film can be grown by metal-organic chemical-vapor-deposition method, volatile surfactant-assisted metal-organic chemical-vapor-deposition method, pulsed-laser depositions method, and rf magnetron sputtering method.